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U.S. PATENT APPLICATION

for

METHOD OF ENHANCING GATE PATTERNING PROPERTIES WITH REFLECTIVE HARD MASK

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. patent Application No. _____, Attorney Docket No. 39153/366 (F0807), entitled USE OF SILICON CONTAINING IMAGING LAYER TO DEFINE SUB-RESOLUTION GATE STRUCTURES, and U.S. Patent Application No. _____, Attorney Docket No. 39153/367 (F0808), entitled BI-LAYER TRIM ETCH PROCESS TO FORM INTEGRATED CIRCUIT GATE STRUCTURES, both of which are assigned to the same assignee as this application and are filed on an even day herewith.

FIELD OF THE INVENTION

[0002] The present specification relates generally to integrated circuits and methods of manufacturing integrated circuits. More particularly, the present specification relates to enhancing gate patterning properties with reflective hard mask.

BACKGROUND OF THE INVENTION

0003] Semiconductor devices or integrated circuits (ICs) can include millions of devices, such as, transistors. Ultra-large scale integrated (ULSI) circuits can include complementary metal oxide semiconductor (CMOS) field effect transistors (FET). Despite the ability of conventional systems and processes to fabricate millions of IC devices on an IC, there is still a need to decrease the size of IC device features, and, thus, increase the number of devices on an IC.

[0004] One limitation to achieving smaller sizes of IC device features is the capability of conventional lithography. Lithography is the process by which a pattern or image is transferred from one medium to another. Conventional IC lithography uses ultra-violet (UV) sensitive photoresist. Ultra-violet light is projected to the photoresist through a reticule or mask to create device patterns on an IC. Conventional IC lithographic processes are limited in their ability to print small features, such as contacts, trenches, polysilicon lines or gate structures.

[0005] Generally, conventional lithographic processes (e.g., projection lithography and EUV lithography) do not have sufficient resolution and accuracy to consistently fabricate small features of minimum size. Resolution can be adversely impacted by a number of phenomena including: diffraction of light, lens aberrations, mechanical stability, contamination, optical properties of resist material, resist contrast, resist swelling, thermal flow of resist, etc. As such, the critical dimensions of contacts, trenches, gates, and, thus, IC devices, are limited in how small they can be.

[0006] Another difficulty arising from the continuing small dimensions involved in the creation of gate structures is the tendency in the lithography process to experience resist erosion and pattern collapse during trim etch processes. During trim etch processes, a significant amount of the resist is normally etched away in a vertical direction, resulting in a substantial weakening and thinning of the photoresist. This significant reduction of the vertical dimension or thickness of the photoresist from its untrimmed vertical dimension can promote discontinuity thereof, resulting in the photoresist being incapable of providing effective masking in the fabrication of the gate. The resist thickness erosion occurs during etch processes. Exemplary trim

processes are described in U.S. Patent No. 5,965,461 entitled CONTROLLED LINEWIDTH REDUCTION DURING GATE PATTERN FORMATION USING A SPIN-ON BARC.

[0007] Thus, there is a need to optimize gate patterning and generate a hard mask to control gate final sizes. Further, there is a need for a method of enhancing gate patterning properties with reflective hard mask. Yet further, there is a need to use imaging layers to define gate structures having small critical dimensions.

SUMMARY OF THE INVENTION

0008] An exemplary embodiment is related to a method of fabricating an integrated circuit. This method can include depositing a reflective metal material layer over a layer of polysilicon, depositing an anti-reflective coating over the reflective metal material layer, trim etching the anti-reflective coating to form a pattern, etching the reflective metal material layer according to the pattern, and removing portions of the polysilicon layer using the pattern formed from the removed portions of anti-reflective coating.

[0009] Another exemplary embodiment is related to a method of optimizing optical properties of gate patterning to control gate size in an integrated circuit fabrication process. The method can include providing a reflective metal layer over a gate material layer, providing a mask layer over the reflective metal layer, and patterning the gate material layer including selectively etching the mask layer and the reflective metal layer.

[0010] Another exemplary embodiment is related to a method of forming a gate in an integrated circuit. This method can

include providing a gate material layer, providing a reflective metal layer over the gate material layer, providing an anti-reflective coating (ARC) layer over the reflective metal layer, providing a resist layer over the ARC layer, and patterning a gate structure in the gate material layer by selectively removing portions of the resist layer, ARC layer, and gate material layer.

[0011] Other principle features and advantages of the invention will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0013] FIGURE 1 is a schematic cross-sectional view representation of a portion of an integrated circuit fabricated in accordance with an exemplary embodiment;

[0014] FIGURE 2 is a schematic cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 1, showing a deposition step;

[0015] FIGURE 3 is a schematic cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 2, showing an etching step; and

[0016] FIGURE 4 is a perspective cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 3, showing a gate structure formation step.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0017] With reference to FIGURE 1, a portion 110 of an integrated circuit (IC) includes a transistor 112 which is disposed on a semiconductor substrate 114, such as, a wafer. Semiconductor substrate 114 is preferably a bulk P-type single crystalline (001) silicon substrate. Alternatively, substrate 114 can be an N-type well in a P-type substrate, an insulative substrate, a semiconductor-on-insulator (SOI) substrate, (preferably silicon-on-glass) or other suitable material for transistor 112.

[0018] Transistor 112 can be a P-channel or N-channel metal oxide semiconductor field effect transistor (MOSFET). Transistor 112 is preferably embodied as a MOSFET and includes a gate structure 118, a source region 122, and a drain region 124. Gate structure 118 advantageously includes single crystalline material that reduces variability in gate lengths due to grain structure. In one embodiment, gate structure 118 has a gate length between source region 122 and drain region 124 in the nanometer scale.

[0019] For an N-channel transistor, regions 122 and 124 are heavily doped with N-type dopants (e.g., $5x10^{19}$ – $1x10^{20}$ dopants per cubic centimeter). For a P-channel transistor, regions 122 and 124 are heavily doped with P-type dopants ($5x10^{19}$ - $1x10^{20}$ dopants per cubic centimeter). An appropriate dopant for a P-channel transistor is boron, boron diflouride, or iridium, and an appropriate dopant for an N-type transistor is arsenic, phosphorous, or antimony.

[0020] Source and drain regions 122 and 124 can be provided with extensions 123 and 125. Preferably, ultra-shallow extensions 123 and 125 (e.g., junction depth is less than 20 nanometers (nm), 100-250Å) are integral with regions 122 and 124. Source and

drain extensions 123 and 125 can be disposed partially underneath gate structure 118.

[0021] A channel region 141 underneath gate structure 118 separates regions 122 and 124. Region 141 can be doped according to device parameters. For example, region 141 can be doped according to a super steep retrograded well region.

[0022] Gate stack or structure 118 includes a gate conductor 136 and a gate dielectric layer 134. Alternatively, structure 118 can include three or more conductive or semiconductive layers.

[0023] Gate conductor 136 is preferably a polysilicon material. Gate conductor 136 has a thickness of 800—1600 Å and a width of less than 50 nm (e.g., channel length). Conductor 136 can have a width that is less than the width achievable by conventional lithography.

[0024] Gate conductor 136 can be a semiconductor material implanted with dopants, with other semiconductive materials or can be an in situ doped material. Gate conductor 136 is also preferably heavily doped with an N-type dopant, such as phosphorous (P), arsenic (As) or other dopant. Alternatively, gate conductor 136 can be doped with a P-type dopant, such a boron (B), boron diflouride (BF_2), or other dopant.

[0025] Dielectric layer 134 is preferably a 15 to 25 Å thick thermally grown silicon dioxide layer. Alternatively, layer 134 can be a silicon nitride layer. Dielectric layer 134 can be comprised of a high-k dielectric material such as a 2-10 nm thick conformal layer of tantalum pentaoxide (Ta_2O_5), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2) or other material having a dielectric constant (k) over 8.

[0026] A silicide layer can be disposed above source region 122, drain region 124, and conductor 136. Preferably, a nickel silicide (WSi_x) is utilized. Alternatively, the silicide layer can be any type of refractory metal and silicon combination, such as, a cobalt silicide, tungsten silicide, titanium silicide, or other silicide material.

[0027] Transistor 112 can be an N-channel or a P-channel field effect transistor, such as, a metal oxide semiconductor field effect transistor (MOSFET). Transistor 112 is at least partially covered by insulative layer 148 and is preferably part of an ultra-large scale integrated (ULSI) circuit that includes one million or more transistors.

[0028] Spacers 162 are preferably silicon nitride spacers and have a height of 800—1600 Å and a width of 400—600 Å. Spacers 162 abut side walls of conductor 136 and layer 134.

[0029] With reference to FIGURES 1-4, the fabrication of transistor 112, including gate conductor 136 is described as follows. The advantageous process allows gate structure to have a small critical dimension, such as, width. The width of conductor 136 can be related to the gate length of transistor 112. Further, the process described with respect to FIGURES 1-4 optimizes gate patterning and generates a hard mask to control gate final size.

[0030] Referring to FIGURE 2, a schematic cross-sectional view representation of a portion 210 of an integrated circuit (IC) includes a polysilicon layer 212, a reflective metal layer 214, an anti-reflective coating (ARC) layer 216, and a resist layer 218. Portion 210 is preferably part of an ultra-large-scale integrated (ULSI) circuit having millions or more transistors. Portion 210 is manufactured as part of the IC on a semiconductor wafer, such as, a silicon wafer.

[0031] Polysilicon layer 212 can be any of a variety of materials which can serve as a portion of a gate structure 118 (FIGURE 1). In an exemplary embodiment, polysilicon layer has a thickness between 500 and 2500 Angstroms (preferably, 1,000 Angstroms, for example). Alternatively, layer 212 can be other materials suitable for gate conductor 136. Layer 212 can be a refractory metal or a single crystalline material. Layer 212 can be in-situ doped or doped subsequently. In one embodiment, layer 212 is an 800-1600 Angstroms polycrystalline layer deposited by chemical vapor deposition (CVD) or a 800-1600 Angstrom aluminum layer deposited by sputter deposition.

[0032] Reflective metal layer 214 can be tungsten (W) or any other reflective metal. ARC layer 216 can be SiN, SiON, SiRN, or any other suitable material having appropriate anti-reflective properties. ARC layer 216 is located above reflective metal layer 214 and polysilicon layer 212. In an exemplary embodiment, ARC layer 1216has a thickness of 400-800 Angstroms and reflective metal layer 214 has a thickness of 80-200 Angstroms.

[0033] In an exemplary embodiment, reflective metal layer 214 is deposited on polysilicon layer 212. ARC layer 216 is deposited over reflective metal layer 214. Resist layer 218 is then provided over ARC layer 216. In an exemplary embodiment, reflective metal layer 214 is deposited using a chemical vapor deposition (CVD) application of a thin tungsten material. In an exemplary embodiment, reflective metal layer 214 containing tungsten has a thickness of 80-200 Angstroms. ARC layer 216 is deposited in a CVD or spin-on process. Resist layer 218 can be applied by a spin coating process.

[0034] Patterning of ARC layer 216 can be done using a variety of techniques, such as, photolithography or e-beam lithography.

Such patterns can be transferred from resist layer 218. In an exemplary embodiment, resist layer 218 is patterned via radiation and developed. Then, ARC layer 216 is etched in accordance with resist layer 218 and resist layer 218 is removed.

[0035] After layer 216 is patterned from resist layer 218, portion 210 is exposed and developed. Referring now to FIGURE 3, an isotropic etch is applied to remove portions of reflective metal layer 214. In an exemplary embodiment, a trim etch technique is employed to undercut ARC layer 216. As such, reflective metal layer 214 has a pattern with smaller widths than ARC layer 216. During the underlayer etch, ARC layer 216 is stripped. Advantageously, the pattern created includes widths which are less than one lithographic feature. ARC layer 216 is stripped using an etching process or, alternatively, a hydrofluoric acid (HF) dip. The etching process can be a wet or dry etch consistent with industry practice. This etch results in a rounded shape to remaining portions of reflective metal layer 214, as shown in FIGURE 4.

[0036] Referring now to FIGURE 4, polysilicon layer 212 is selectively etched using remaining portions of reflective metal layer 214 as a hard mask pattern. Remaining portions of polysilicon layer 212 can serve as gate structures 232. Advantageously, gate structures 232 have a width or critical dimension which are not limited by the lithography processes but other fabrication limitations. Gate structures 232 correspond to gate structure 118 described with reference to FIGURE 1.

[0037] Referring again to FIGURE 1, source and drain regions 122 and 124 are formed in substrate 114, extensions 123 and 125 are formed, a silicide layer is deposited, and spacers 162 are provided. In another exemplary embodiment, additional features are formed during the integrated circuit fabrication process.

[0038] Advantageously, deposition of a thin reflective metal, such as, tungsten (W) followed by an anti-reflective coating (ARC), such as, SiON and then resist optimizes optical properties of gate patterning. Reflective metal layer 214 is optically opaque to polysilicon layer 216. As such, the thickness of polysilicon layer 216 is unaffected by the use of reflective metal layer 214. In contrast, an anti-reflective coating (ARC) used alone must be matched to the polysilicon or gate layer material.

[0039] Gate stack or structure 118 can be patterned using SiON layer 210 and reflective metal layer 214. In an exemplary embodiment, metal layer 214 has very good selectivity to polyetch. As such, metal layer 214 holds up well even though a large trim of ARC layer 216 reduces the thickness of metal layer 214. However, metal layer 214 only needs to be a few 100 Angstroms to withstand the etch. Advantageously, due to etch chemistry differences in films, good selectivity can be achieved between the ARC layer, reflective metal layer, and the polysilicon gate layer.

[0040] While the exemplary embodiments illustrated in the figures and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. Other embodiments may include, for example, different methods of patterning or etching various layers as well as different methods of application of ARC layer 216. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that nevertheless fall within the scope and spirit of the appended claims.